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A NOVEL VOLTAGE-MODE LUT USING CLOCK BOOSTING TECHNIQUE IN STANDARD CMOS

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***Abstract*: In a VLSI circuit, interconnection plays the dominant role in every part of the circuit nearly 70 percent of the area depends on interconnection, 20 percent of the area depends on insulation, and remaining 10 percent to devices. The binary logic is limited due to interconnect which occupies a large area on a VLSI chip. In this work, the designs of quaternary-valued logic circuits have been explored over multi-valued logic due to the following reasoning. An approach to mitigate the impact of interconnections is to use multiple-valued logic (MVL), hence, more information can be carried in each wire, reducing the routing network. Therefore, a single wire carrying a signal with N logic levels can replace [$\log_2$N] wires carrying binary signals. Reducing the routing leads to a direct reduction of the line capacitance and the overall circuit area. Therefore, this results in increasing the maximum operation frequency and also reducing the power consumption. The most important characteristics of this method are a voltage-mode structure. Voltage mode structure has the advantages like reduced power consumption implemented in a standard CMOS technology. Our new method overcomes convectional techniques with simple and efficient CMOS structures.**

***Keywords:* Multiple-value Logic, Quaternary logics, Look- up tables, FPGAs, Standard CMOS Technology**

I. INTRODUCTION

Power dissipation mainly occurs due leakage current and static power dissipation and has formula

$$P_d \propto CV^2_{dd}$$

Therefore by reducing the capacitance value we can able to reduce the dissipation.one of the important advantage of quaternary logic is that has the reduced noise margin when compared to the conventional binary logic. More over if we use the current mode we have to face the problem in the fabrication process and has the high power consumptions.

II. BINARY AND QUATERNARY LOOK-UP TABLES

In General Look-Up Tables (LUT) are basically memories, which implement a logic Function according to their configuration. Configuration values C = (c0….. ci, c_{k-1}); are initially stored in the look-up table structure, and once inputs are applied to it, the logic value in the addressed position is assigned to the output.

The capacity of a LUT |C| is given by

$$|C| = n \times b^k \qquad (1)$$

Where n denotes the number of outputs, k denotes the number of inputs and b for the number of logic values. For example, a 4-input binary look-up table with one output is able to store $1 \times 2^4 = 16$ Boolean values.

A binary function implemented by a Binary Look-Up Table (BLUT) is defined as f: $B^k \rightarrow B$, over a set of variables X = (x0,…xi,…. ; x_{K-1}), where each variable xi represents a Boolean value. The total number of different functions |F| that can be implemented in a BLUT with k input variables is given by

$$|F| = b^{|C|} \qquad (2)$$

Where b = |B| (b = 2 in the binary case). For example, a look-up table with 4 inputs (k = 4) can implement one of |F| = 65,536 different functions. Quaternary functions are basically generalizations from binary functions. This function implemented by a quaternary look-up table (QLUT) is defined as g: $Q^k \rightarrow Q$, over a set of quaternary variables Y = (y0,….. yi …… y_{k-1}), where the values of a variable yi, as the values of the function g(Y), can be in Q= {0,1,2,3}. As in the binary case, the number of possible function in QLUTs is given by (2), where b = 4. In this case, the number of functions that can be represented is everywhere 4.3×10^9 for a QLUT with only two quaternary inputs (k = 2), which is much larger than for the BLUT.

The quaternary variable y is capable of representing twice as much information as a binary variable x, we note that the cardinality of |Q| = 2 × |B| in our experiments. In other words, two binary variables with the same inputs can be grouped in order to represent a quaternary variable. Such procedure mainly for reducing both the total number of connections and the number of gates.

III. QUATERNARY LOGIC AND REFERENCE VOLTAGES LEVELS.

This design was implemented using a standard CMOS technology, a single supply voltage and a clock boosting technique to incorporate a 16 to 1 multiplexer and a dual quaternary decoder. One of the most important feature that was taken into account was the area usage since that, in order to perform more complex functions, this circuit needs to be replicated a millions of times in the FPGA

The circuit depicted in the table below has two quaternary inputs, QA and QB, which are then computed by the dual quaternary decoder into the QLUT's binary control signals, B00-B33. The multiplexer 16-to-1 consists of sixteen NMOS switches enhanced with a clock boosting technique. When one of the control signals is high, the corresponding QLUT's line- switch- is activated connecting the corresponding QLUT's quaternary input to the output.

The four voltage levels are represented on table

Table 1: The four voltage levels

value	Voltage value [v]
0	0
1	0.404
2	0.707
3	1.2

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, 1⁄6*V*DD, 3⁄6*V*DD, and 5⁄6*V*DD, to determine a quaternary value.

A LUT is an array indexing operator, where the output is mapped by the input, based on the configuration memory. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic value in the addressed position is assigned to the output.

IV. 16-1 MUX

A Multiplexer has many inputs and one output has to be selected. Although, the Use of quaternary logic helps to reduce the number of interconnecting wires, which leads to a compact layout, with reduced routing capacitance. We used the typical value for a binary FPGA (10 pF), since it maintain same number of wires, we can increase the number of functions in FPGA.

When compared to binary quaternary implementation of 16-1 multiplexer quaternary had the least number of gates. For the binary implementation nearly 30 transmission gates are used but in case of quaternary only 24 transmission gates are used.

Table 2: Quaternary and binary input table

BINARY					QUATERNERY		
DC	8	4	2	1	DC	**4**	**1**
0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	1
2	0	0	1	1	2	0	0
3	0	1	0	0	3	0	1
4	0	1	0	0	4	1	0
5	0	1	0	1	5	1	1
6	0	1	1	0	6	1	0
7	0	1	1	1	7	1	1
8	1	0	0	0	8	2	0
9	1	0	0	1	9	2	1
10	1	0	1	0	10	2	0
11	1	0	1	1	11	2	1
12	1	1	0	0	12	3	0
13	1	1	0	1	13	3	1
14	1	1	1	0	14	3	0
15	1	1	1	1	15	3	1

IV.1 Clock Boosting Techniques

Clock boosting techniques is the important technique for reducing the interconnection problems and increase the speed with reduced delays.

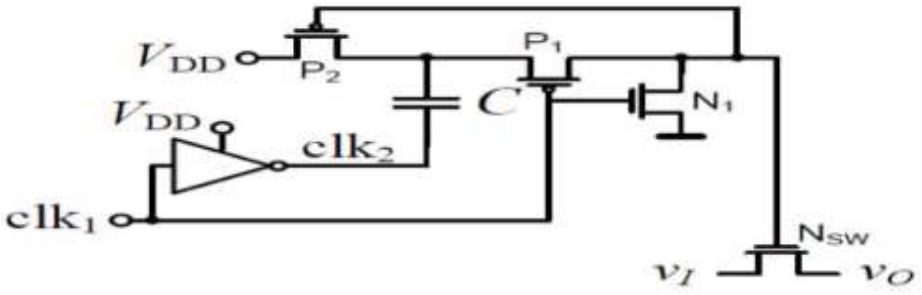

Fig.1. Proposed transistor-level schematic

Assuming that the capacitor *C* is discharged and clk1 is set to logic 1 (*V*DD), *N*1 turns on and connects node B to ground, while *P*1 turns off and ensures a high impedance path between the nodes A and B. Simultaneously, *P*2 is on and gradually charges the capacitor (and node A) to *V*DD. When clk1 commutes to a logic 0 (ground), *N*1 turns off; the inverter ties the capacitor bottom plate to *V*DD and *P*2 turns off; node Arises to 2*V*DD and *P*1 is turned on connecting node B to 2*V*DD as wanted.

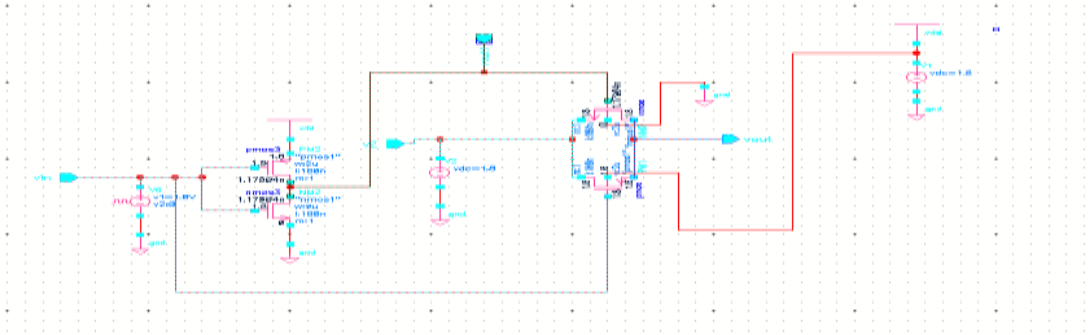

Fig 2: Transmission gate diagram

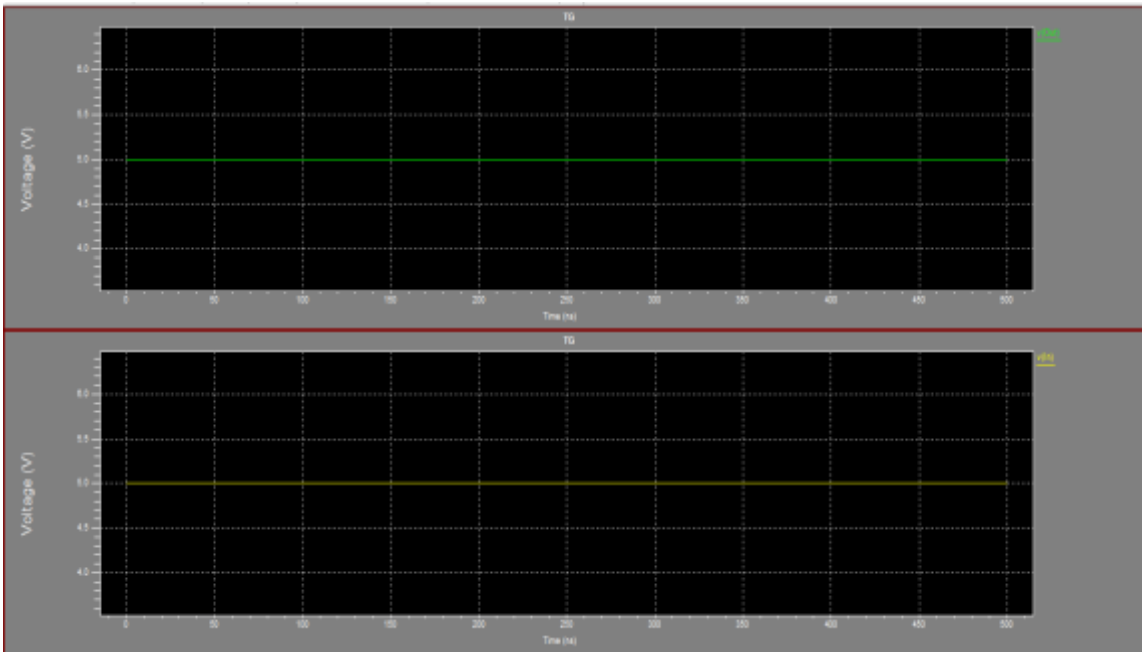

Fig 3: Transmission gate output

V. 16-1 MUX USINS TRASMISSION GATES

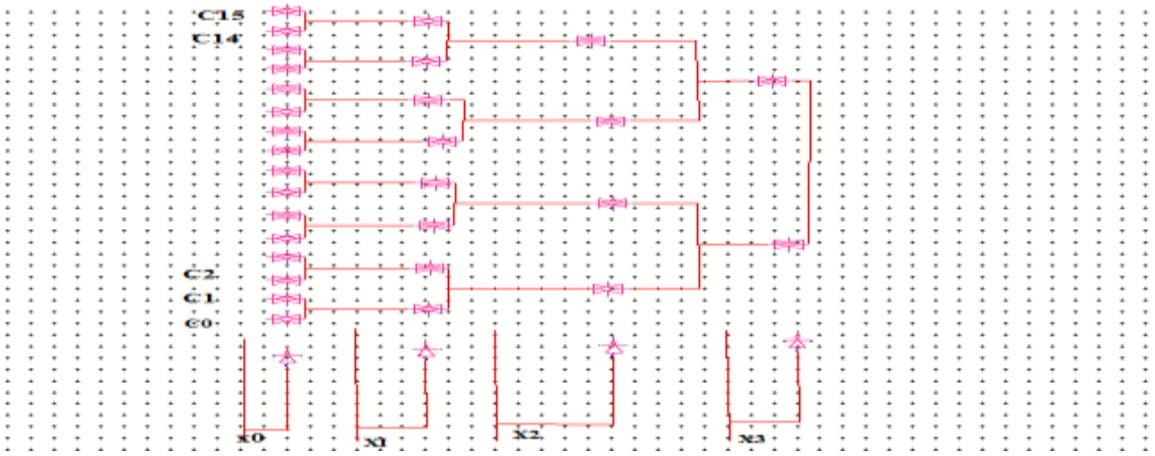

Fig 4: Binary 16-1 mux

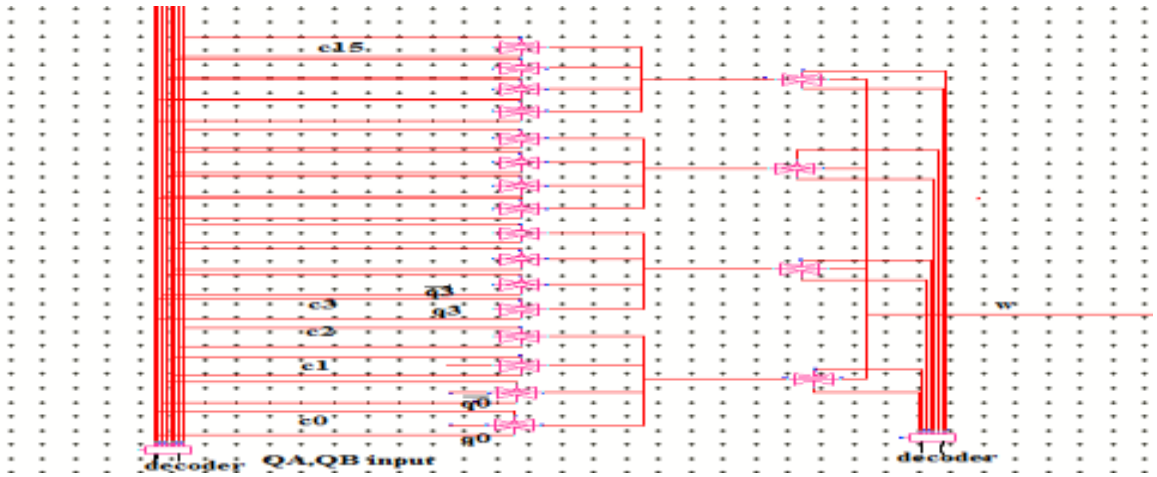

Fig 5: Quaternary 16-1 mux

VI. QUATERNARY-TO-BINARY CONVERTER

Table 3: The Q-decoder behavior as a function of the quaternary logic value at the input

Q	Q_0	Q_1	Q_2	Q_3
0_4	1_2	0	0	0
1_4	0	1_2	0	0
2_4	0	0	1_2	0
3_4	0	0	0	1_2

From the above table it shows the binary output as the function of quaternary input. Here Q0, Q_1, Q2, Q3 are the binary values meaning 0 (0V) or 12 (VDD).and q is the quaternary logic.

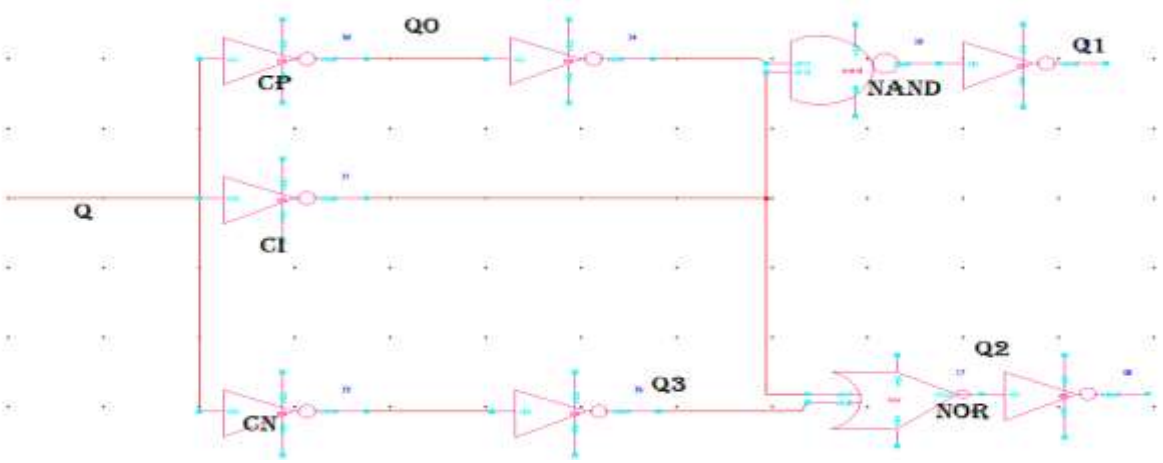

Fig 6: The Q-decoder logic structure.

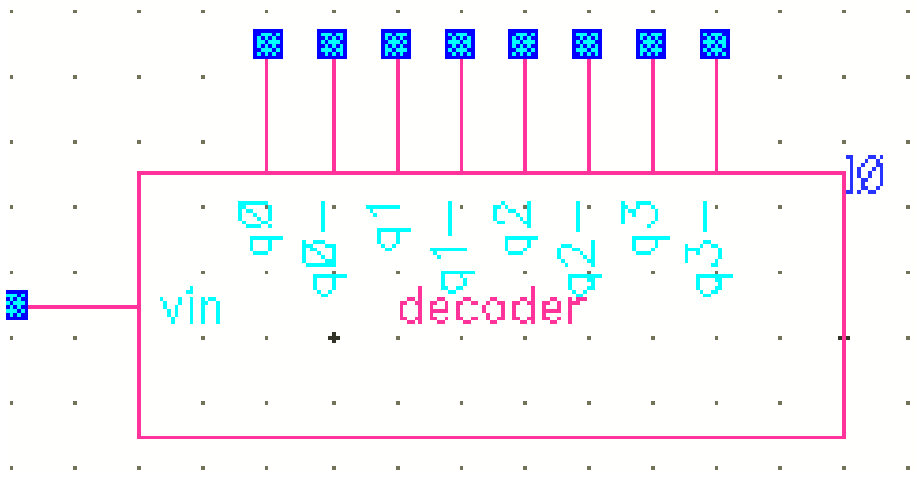

Fig 7: Symbol creation for decoder

The main advantage of this structure compared to previous proposed implementations is that it has standard CMOS structures. The Q-decoder is composed of two comparators CP and CN, and other traditional digital circuits inverters, NANDs and NORs.The CP and CN are self-reference analog comparators shown in Fig. 3. With these structures we are able to detect the four possible voltage levels. In a binary implementation, an inverter may be seen as a comparator where the voltage reference is VDD=2. For our quaternary device, we need three voltage references in order to determine a quaternary value, at 1/6VDD, 3/6VDD and 5/6VDD, as depicted in Figure given below

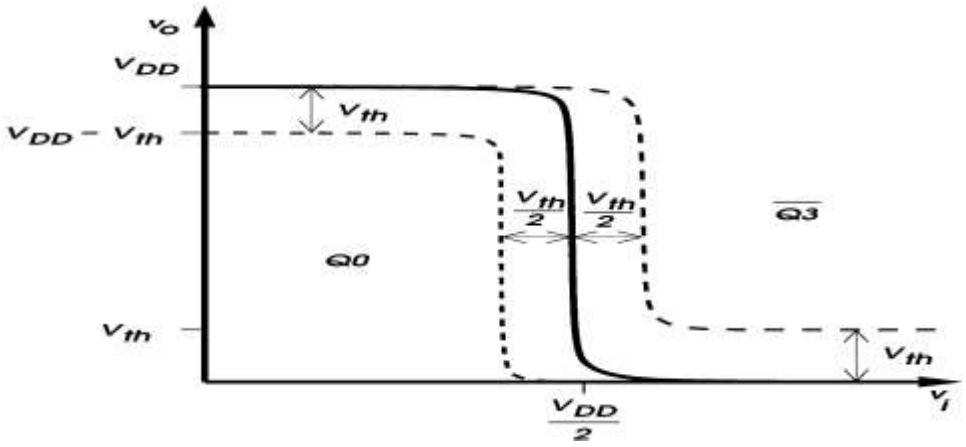

Fig 8: CP and CN transfer functions.

Thus first for design of decoder we need to design the three CP, CI,CN .CI is the inverter with the input 1 to get output 0.

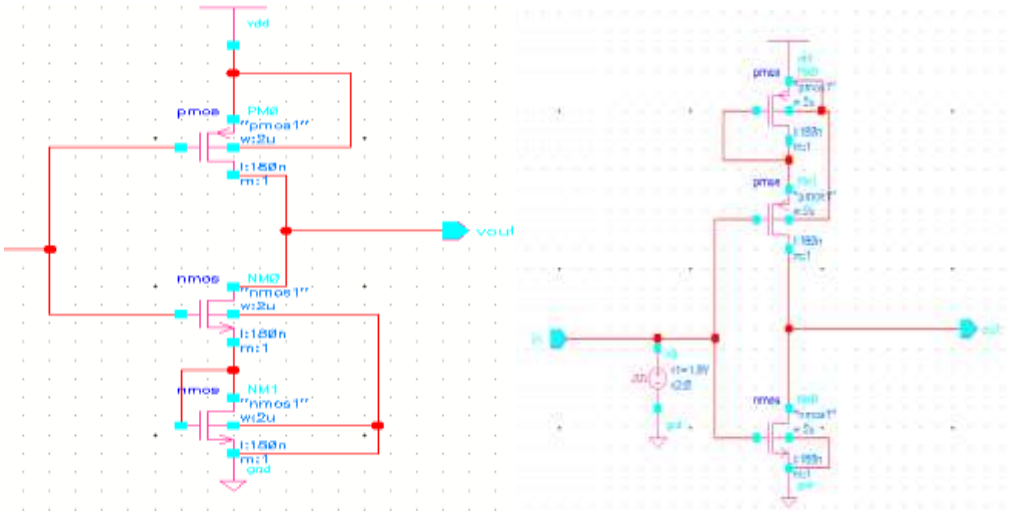

Fig 9: a)Cp diagram **b) CN diagram**

We also implemented the complete binary and quaternary look-up tables with the UMC 130nm technology in order to evaluate their performance and power consumption. The development of the binary and quaternary LUTs was performed . Transistor widths were kept to the minimum value in order to have a fair comparison between binary and quaternary versions.

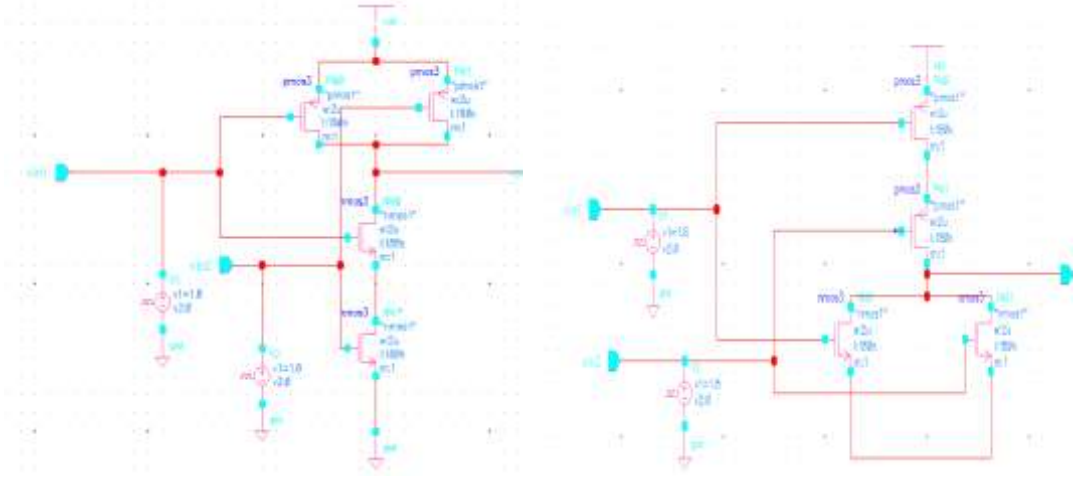

Fig 10: a) NAND GATE **b) NOR GATE**

VII. Q-DECODER INPUTS AND OUTPUTS WAVEFORMS WITH COMPARISON TABLE

The quaternary structure proposed in this paper outperforms the binary implementation in both power Consumption and propagation delay. These results were obtained through CADENCE Spectra simulation. The propagation delay is simply the largest delay from an input to the output of each LUT.

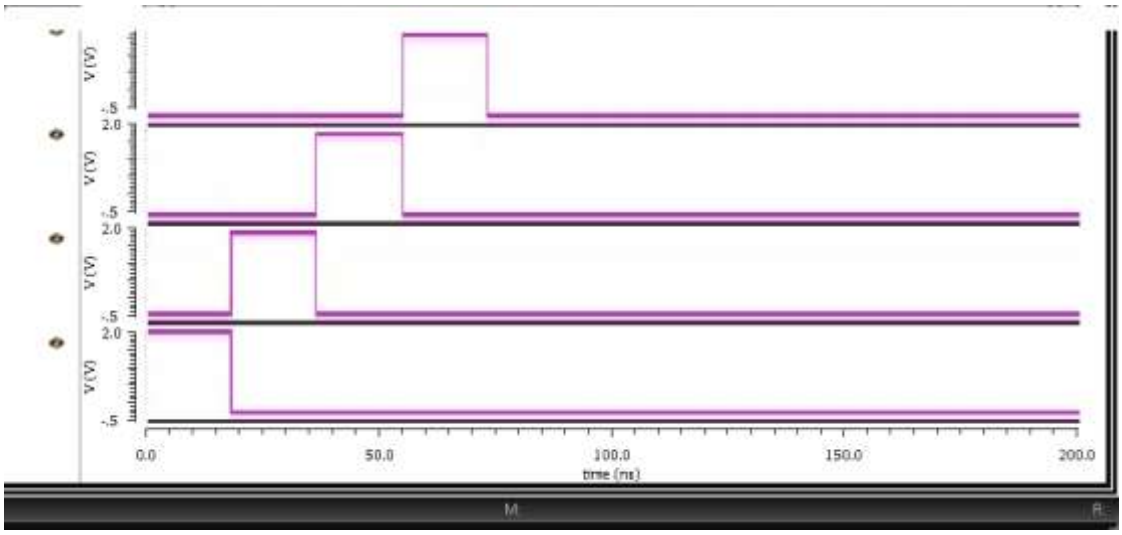

Fig 11: The Q-decoder outputs waveforms.

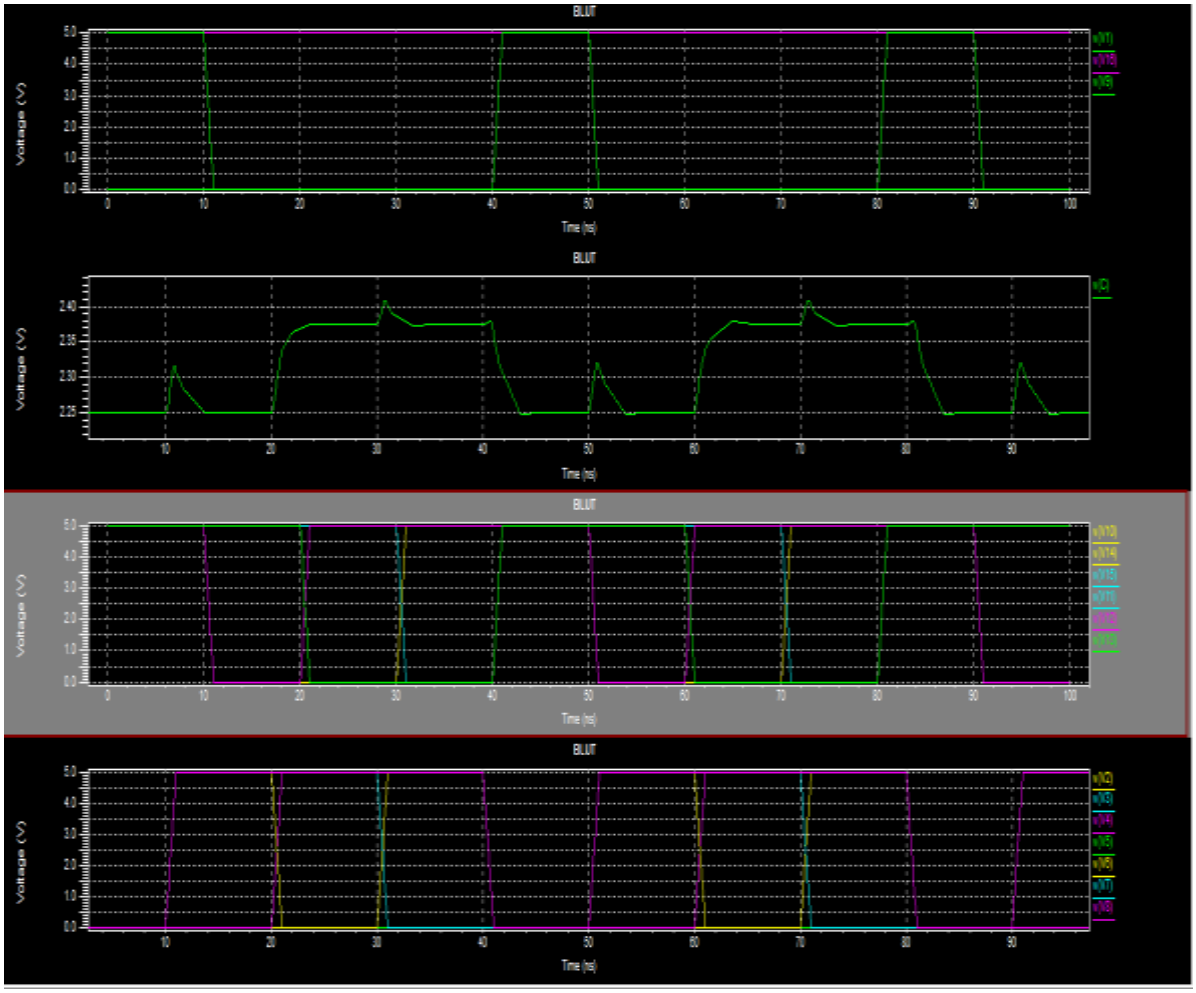

Fig 12: Quaternary 16-1 mux output

TABLE 4: COMPARISON WITH STATE-OF-THE-ART LUTS BINARY

	THIS WORK	PAPER 13	PAPER 14	PAPER 8	PAPER 14	PAPER 9
NUMBER OF INPUTS	2	2	2	2	5	4
TECHNOLOGY NODE	UMC 130nm	UMC 130nm	TMSC 130nm	TSMC 180nm	TSMC 180nm	UMS 130nm
TECHNIQUE	STD CMOS	STANDARD CMOS	3 DIFFERENT VTH	3 DIFFERENT VTH	STANDARD CMOS	STANDARD CMOS
SUPPLY VOLTAGE	1.2V	1.2V	1.2V	3 V	3 V	1.8 V
FREQUENCY	100MHz	100MHz	1MHz	500 MHz	1GHz	100 MHz
RISE/FALL TIME	1.5ns	5 ns	0.9 ns	0.50 ns	1.07 ns	3 ns
TRANSITER COUNT	220	112	120	44	236	68
POWER CONSUMPTION	140µW	126µW	134 µW	155µW	450µW	94 µW

VIII. CONCLUSION

In this paper, we have reported an innovative QLUT design that can be used for multiple valued combinational logic or as a building block in FPGAs. The QLUT internal functionality is implemented using simple standard CMOS structures. This feature is achieved through quaternary-to-binary decoders that quantize the input signals. This decoder is based on voltage-mode self-referenced comparators that allows the use of a standard CMOSTechnology and overcomes previous design drawbacks. Also, a CB technique was used to decrease the switches resistance and increase the operation frequency, while at the same time, achieving low power consumption. Therefore, the presented design is a valid solution to reduce the interconnections impact, without increasing Power consumption or losing performance. Experimental results were performed on an ASIC implementation of a full adder employing the designed QLUT. The obtained results attested the circuit feasibility and its advantages, using a standard CMOS process and its main characteristics (timing and power)

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